Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to include Examiners noted grammatical errors and Examiners suggestions are gratefully acknowledged by Applicants. Applicants have additionally corrected additional grammatical errors.

Claims have been amended to clarify Applicants disclosed and claimed invention as suggested by Examiner to overcomes Examiners rejection of claims 1 and 16 under 35 USC section 112, first paragraph, and Examiners objections to claims 1 and 11 as well as amendments to correct grammatical errors. Claims 1 and 11 have additionally been amended to make clear that the patterned photoresist layer comprises an opening. Support for the amended and newly presented claims is found in the original claims and/or Specification and are in response to Examiners suggestions/ requirements. No new issues have been presented and no new matter has been entered.

Claim Objections

Claims 1-4, 8, 10-19, and 21-14 have been objected to by Examiner.

Applicants have amended claims 1 and 11 to overcome Examiners rejection in accordance with Examiners suggestion/requirement to make clear that the patterned photoresist layer comprises an opening. In addition, claims 1 and 11 have been amended to correct grammatical errors.

Claim Rejections under 35 USC 112

Claims 1-4, 8, 10, and 21-22 stand rejected under 35 USC 112, first paragraph as failing to comply with the written description requirement.

Applicants have amended claim 1 to recite a single passivation layer as suggested/required by Examiner. Applicants have amended claims 1 and 11 to further make clear that the patterned photoresist layer comprises the opening consistent with the disclosures and Figures and as suggested/required by Examiner.

Claims 16 stands rejected under 35 USC 112, second paragraph for failing to particularly point out and distinctly claim subject matter which Applicants regard as the invention.

Applicants have amended claim 16 to recite a single UBM layer consistent with antecedent basis in the claim.

Claim Rejections under 35 USC 103(a)

1. Claims 1-4, 8, 10-19, and 21-24 stand rejected under 35 USC 103(a) as being unpatentable over Costas et al. (U.S. Patent 6,137,125) in view of admitted prior art and further in view of Lee (US U.S. Patent 6,410,414)

Costas et al. disclose a 2-layer hermetic coating for on wafer encapsulation of GaAs monolithic microwave integrated circuits (MMIC) using benzocyclobutene (BCB) and ceramic materials for the coating to provide both mechanical protection and protection from moisture to the MMIC (see Abstract; col 2, lines 21-30). Costas et al. teach that the benefit of using BCB in the hermetic coating includes a low dielectric constant useful for capacitive decoupling of the underlying MMIC (see col 2, lines 33-44) as well as "reducing stress between the carrier and the substrate that often occurs during flip-chip mounting" (see Abstract).

Costas et al. disclose a method where a BCB (polymer) layer is first formed including removing the BCB layer from all bond pads and streets (exposed areas of an implanted portion of GaAs wafer or other semi-insulating surface - see Figure1, col 3, lines 34-45), forming an overlying ceramic layer, followed by patterning a photoresist layer over the ceramic layer, followed

by RIE etching to expose bonding pads (see col 3, lines 47-67) and surrounding areas (see Figure 3).

In contrast, in Applicants disclosed and claimed invention, Applicants claim forming a protective layer (e.g., resinous organic layer with a particular Tg, e.g., BCB) over a UBM (metal) layer, forming a patterned photoresist layer on the protective layer where the patterned photoresist layer comprises an opening overlying the UBM layer; and forming a solder column within the opening (following removal of the protective layer over the UBM layer at the bottom of the opening as specifically claimed in independent claim 11 and dependent claim 21), followed by a first solder reflow process (and second solder reflow process after removal of remaining photoresist and protective layer in claims 11 and 21).

Significantly, Applicants disclosed and claimed invention teaches removing remaining portions of the protective layer following the first solder reflow prior to a second solder reflow to form a solder ball (see dependent claim 21 and independent claim 11).

In contrast, in the method of Costas, et al., the protective layer (e.g., BCB, low dielectric constant polymer) is removed

over portions (e.g., bond pads and surrounding areas) prior to **forming an overlying ceramic layer** and a patterned photoresist layer over the ceramic layer. In addition, portions of the protective layer (BCB layer) **remain in place,** becoming part of the device (see e.g., col 2, lines 30-44, col 5, lines) 12 15) as a capacitive decoupling encapsulating material. Moreover, Costas discloses forming solder bumps using an electroplating method and does not disclose Applicants claimed method which would likely not work with the method of Costas et al.:

"forming a solder column within the opening on the UBM contact layer; and,

"subjecting the solder column with the patterned photoresist in place to a first reflow temperature."

Applicants respectfully suggest that Examiner is clearly mistaken that the disclosure of Costas et al. is "equivalent to forming of solder columns through a patterned resist stencil either (1) of photosensitive BCB or (2) with underlying non-photosensitive BCB, which has been patterned through the resist stencil." Examiner provides no support for this assertion.

The method of Costas et al. works by a different principal of operation than Applicants disclosed and claimed invention.

The solder bumps of Costas et al. could likely not be formed within a patterned photoresist opening as claimed by Applicants since the thickness (height) of the BCB layer of Costas et al. is about as thick as the height of the solder bumps and the geometry as shown in Figure 6 appears incompatible with such a process. Likewise the purpose of the method of Costas et al. in using the low dielectric constant polymer (e.g., BCB) as an encapsulant **as part of the completed device** is to reduce capacitive coupling and thermal stresses in a flip chip bonding process which would be obviated by the method of Applicants where the protective layer is subsequently removed (see dependent claims 22 and independent claim 11). Further, the method of Costas et al. does not disclose or contemplate a solder reflow processes with a photoresist layer overlying a protective layer as claimed by Applicants.

Specifically, Costas et al. do not disclose forming a patterned photoresist layer over (on) a protective layer followed by subjecting both the photoresist (and solder column formed therein) as well as protective layer portions underlying the photoresist layer (e.g., BCB) to a solder reflow temperature.

Moreover, the Costas et al. do not recognize or suggest a solution to the problem that Applicants invention has recognized

and solved: "A method for protecting a semiconductor process wafer surface from thermally degraded photoresist to improve a solder ball formation process".

Examiner cites Applicants for admitted prior art put forth in the background of the invention to outline the problem presented and solved by Applicants claimed invention. Applicants respectfully suggest that Examiner is improperly finding motivation for combining Costas et al. with Applicants state of the prior art gleaned solely from Applicants disclosure where a problem in the prior art is presented and then solved by Applicants disclosed and claimed invention. That is, there is no motivation independent from Applicants disclosure for combining Costas et al. with Applicants disclosure presenting a problem to be solved in the prior art.

Nevertheless, assuming *arguendo* proper motivation for combination, such combination does not produce Applicants claimed invention. Nowhere does Applicants presentation of the problem to be solved or the teachings of Costas et al. suggest, discuss or disclose forming a protective layer which is formed underlying a patterned photoresist layer; forming a solder column within the patterned photoresist layer; and subjecting both the protective layer, photoresist, and solder column to a solder reflow

temperature to solve the problem of protecting a semiconductor process wafer surface from thermally degraded photoresist. Rather, the method of Costas et al. affirmatively and inherently teaches away from Applicants claimed process, operating by a different principal of operation.

Examiner argues that "Costas teach the applicability of an underlying BCB for a process involving subsequent solder bump of column formation". Applicants respectfully point out that Examiner is mistaken. Rather, Costas et al. teach removing the BCB layer over wafer surface portions where a subsequent solder column is formed by an electroplating process. Costas et al. do not disclose or teach a patterned photoresist layer overlying a BCB layer including a solder column subjected to a reflow temperature as Applicants have disclosed and claimed.

Examiner argues that "any judgment on obviousness is in a sense necessarily a reconstruction based on hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and **does not include knowledge gleaned only from the Applicants disclosure**, such a reconstruction is proper; citing *In re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971)*.

However, Applicants respectfully point out that the only disclosure, teaching, suggestion leading to motivation for doing what Applicants have done is solely gleaned from Applicants disclosure of the state of the prior art and in presenting a problem which Applicants disclosed and claimed invention has solved.

Applicants point out that "we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's**

disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

Lee discloses a process whereby a BCB layer having a low water intake rate and an excellent blocking effect against alpha particles is formed between an alpha particle source such as a solder ball and underlying sensitive integrated circuit devices.

Lee teaches a method whereby a BCB layer remaining a part of the completed device is formed to block alpha rays from impacting underlying circuitry portions. In one embodiment, a passivation layer is formed over a bonding pad and the bonding pad exposed,

followed by forming a metal redistribution layer over the passivation layer and exposed bonding pad, followed by forming a BCB layer over the metal redistribution layer (see e.g., col 2, lines 4-15, col 3, lines 34-35), followed by forming openings in the BCB layer to expose the metal redistribution layer, followed by solder ball formation. Lee does not teach a specific method for forming the solder balls and does not disclose forming a solder column including a solder reflow processes on the solder column with the photoresist in place overlying the protective layer (e.g., BCB layer) as claimed by Applicants or an electroplating process as disclosed by Costas et al. Lee also does not disclose forming a protective layer (e.g., BCB layer) and then removing it as claimed by Applicants. Rather, as disclosed by both Costas et al. and Lee, the BCB layer **remains to form a part of a completed device**, thereby teaching away from Applicants disclosed and claimed invention (e.g, see independent claim 11 and dependent claim 21).

Lee further teaches away from Applicants invention by teaching various locations of the BCB layer (item 112 in Figures 4 through 9 which are variously taught as being formed between the metal redistribution layer and the solder ball e.g., Figure 4; having a polyimide layer between the BCB layer and the solder ball, Figure 5, between a polyimide layer and the solder ball,

Figure 6; and, underlying the metal redistribution layer e.g., Figure 8. It is clear that the various embodiments taught by Lee would not work with the method of Costas et al. nor would work to solve the problem of Applicants disclosed and claimed invention.

Moreover, there is no apparent teaching or motivation to combine Lee with Costas et al. or with Applicants disclosed state of the prior art and problem to be solved. For example, the BCB layer of Lee could not function as a capacitive decoupling encapsulant as envisioned by the teachings of Costas et al., nor would the disclosed locations of the BCB layer in Lee et al. accomplish the purpose of Applicants disclosed and claimed invention, particularly as shown in Figures 5 and 8. In addition, the alpha blocking function of the BCB layer in Lee et al. would likely not protect the device of Costas et al. where a large opening I the BCB layer surrounding the bonding pads is formed prior to solder column (as opposed to solder ball) formation.

Nevertheless, even assuming *arguendo*, proper motive for such combination, such combination does not produce Applicants claimed invention nor suggest, recognize, or discuss the problem that Applicants have recognized and solved by their claimed invention. Neither Costas et al., nor Lee disclose a solder

column formation and reflow process as Applicants have claimed. Neither Costas et al. nor Lee disclose exposing a photoresist layer in contact with an underlying protective layer (e.g., BCB) at a solder reflow temperature, such a process being inconsistent with the principal of operation of the methods and structures of both Costas et al. and Lee . Moreover, neither Lee nor Costas et al, teach **removing** the BCB layer prior to a second, solder ball forming, reflow temperature (see e.g., independent claim 11, and independent claim 21), thereby being inconsistent with the principal of operation of Applicants disclosed and claimed invention and destroying the principal of operation of the structures of both Costas et al. and Lee.

The fact that Lee discloses a BCB layer that has a glass transition temperature of 350 °C is not sufficient to make Applicants disclosed and claimed invention *prima facie* obvious.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).*

Applicants respectfully suggest that Examiner has engaged in impermissible hindsight reasoning using knowledge gleaned from Applicants disclosure as a roadmap to recreate Applicants claimed invention. Nevertheless, Examiner has failed to produce Applicants claimed invention by combining the references cited, where such references affirmatively teach away from Applicants disclosed and claimed invention.

Neither Costas et al. nor Lee, in view of the problem in the prior art disclosed by Applicants which Applicants have solved by their disclosed and claimed invention, are sufficient to produce Applicants claimed invention or make out a *prima facie* case of obviousness with respect to Applicants claimed invention.

The claims have been amended in accordance with Examiners suggestions to clarify Applicants invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040